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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/080,985 | 02/22/2002 | Reid James Riedlinger | 10971429-1 | 9993 |

22879 7590 02/28/2005

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| EXAMINER | |
|---|---|
| BRAGDON, REGINALD GLENWOOD | |
| **ART UNIT** | **PAPER NUMBER** |
| 2188 | |

DATE MAILED: 02/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/080,985 | RIEDLINGER ET AL. | |
| | Examiner | Art Unit | |
| | Reginald G. Bragdon | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> --or--
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-4, 10-14, and 19-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Hetherington et al. (5,930,819).

As per claim 1, Hetherington et al. teaches an L2 data cache including 4 address ports ("a plurality of access ports communicatively coupled to said cache memory structure") and 16 banks ("cache memory structure comprising multiple banks"). See figure 5 and column 4, lines 50-52. A memory scheduling window, or MSW 502, is coupled to the tag array and controls access to the L2 cache. All cache memory access that do not hit in the L1 cache will arbitrate and create an entry into MSW 502 (see column 11, lines 61-67). The MSW is organized as a plurality of columns, one for each port, with each column including 32 entries and 4 entries in one row are allowed to launch at the same time. See column 12, lines 24-37. The MSW represents the claimed "queue". A content addressable memory determines inter-row bank conflicts ("circuitry operable to determine bank conflict for pending access requests for said

memory structure"). See column 13, lines 64-67. A picker 606 ("circuitry operable to issue...") is utilized in selecting a row for launching, where the picker is directed to launch one non-conflicting group of accesses every clock cycle. See column 14, lines 22-42.

The picker 606 issues out of order accesses. Hetherington et al. teaches that port 0 is biased such that the access request in the port 0 entry always gains access first. See column 13, lines 55-56. It is taught that when a row comprises multiple accesses and a bank conflict is detected, the picker launches one non-conflicting group of accesses (see column 14, lines 27-31). Assuming the most basic situation where port entry 0 and port entry 1 in a particular row x conflict, then port entry 0 and port entries 2-3 will launch, while port entry 1 will launch on the next cycle. Therefore, entry 1 of row x will be issued out-of-order with the other entries placed in row x.

Furthermore, Hetherington et al. teaches that if the level 2 cache were virtually addressed, the PA fields would be equivalently substituted by virtual address bits ("wherein said circuitry is operable to determine said bank conflict using bits of virtual addresses to be accessed by pending access requests"). See column 13, lines 33-35.

As per claim 11 and 19, these claims are rejected for the reasons set forth for claim 1, above. It is further noted that (for claim 11), in the example set forth above, entry 3 is newer than the entry for entry 1 and will be launched prior to entry 1.

As per claims 19-23, it is noted that by using virtual addresses to address the L2 cache, translation would not be necessary. However, Applicant's claims do not require that translation from a virtual address to a physical address actually occur. In other words, if no virtual address to physical address translation occurs, then the bank conflict is always determined prior to a

complete virtual address to physical address translation. Therefore, Hetherington et al. teaches the limitation of "determining...before a virtual address to be accessed by said pending access request is translated into a physical address..." (claims 19 and 23) and "determine said bank conflict before fully translating said virtual addresses to physical addresses" (claims 21-22).

As per claim 2, Hetherington et al. teaches a bank conflict between at least two entries in a particular row. See column 13, line 64 to column 14, line 6.

As per claims 3 and 10, Hetherington et al. teaches the MSW, where each column can be thought of as a queue serving a particular port. See column 12, lines 31-33. The CAM unit compares all entries in a row (which are "sibling" entries) one clock cycle after insertion in the MSW. See column 13, lines 64-67.

As per claim 4, Hetherington et al. teaches that conflict is between an issued entry (i.e. entry 0) and a pending entry (entry 1).

As per claim 12, Hetherington et al. teaches nominating all entries in a row that do not conflict (plus one entry that may conflict) for accessing the L2 cache. See the discussion for claims 1 and 11, above.

As per claims 13 and 20, Hetherington et al. teaches that the entries in a particular row that will access the L2 cache (i.e. all non-conflicting entries plus one conflicting entry) will be launched during the same cycle, i.e. in parallel. See column 14, lines 30-31.

As per claim 14, Hetherington et al. teaches that the CAM unit compares all entries in a row one clock cycle after insertion in the MSW. See column 13, lines 64-67.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-9, 11-12, and 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rangan (6,711,654) in view of Taylor et al. (5.226,133).

As per claims 1 and 19-20, Rangan teaches a cache memory 107 including a bank array 220 ("multiple banks" or "memory structure") where each bank allows for one access each clock cycle (column 1, lines 21-23). A queue 210 ("means for queuing") stores each access request for the bank array, and multiple ports from the queue may access the bank array ("plurality of access ports") simultaneously ("means for issuing"). See column 1, lines 37-41, and column 3, lines 43-50. Rangan teaches conflict detection unit 240 ("circuitry operable to determine a bank conflict" or "means for determining") which detects multiple requests in queue 210 to access the same bank in the bank array. See column 4, lines 21-23. Rangan further teaches that entries in the queue may access the bank array in an out-of-order mode ("circuitry operable to issue at least one access request to said cache memory structure out of the order it was requested, responsive to a determination of said bank conflict" or "means for nominating"). See column 3, lines 47-50.

Rangan does not teach determining bank conflict using virtual address bits instead of physical address bits. Rangan teaches accessing the L2 cache using physical addresses. Taylor et al. teaches a virtual cache, where the cache is accessed using virtual address bits instead of physical address bits. See column 2, lines 25-27. It would have been obvious to one of ordinary

skill in the art to have modified Rangan to utilize a virtually accessed, L2 cache because Taylor et al. teaches that a virtual cache eliminates the need for a TLB in the cache of a cache hit, thus speeding up the memory access operation since the TLB translation does not need to be done before going to the cache. See column 2, lines 27-30.

As per claim 2, Rangan teaches that the bank conflict is between at least two requests. See column 4, lines 21-23.

As per claim 3, Rangan teaches a queue 210 which stores each access request for the bank array. See above for claim 1. Rangan also teaches comparing a new request for entry in the queue to existing queue entries. See column 4, lines 30-32.

As per claims 5 and 8, Rangan teaches a pipeline, where one type of instruction is completed in stage X and another type of instruction is completed in stage X+2 ("a predefined pipeline...having a plurality of stages with one stage for performing a first type of access and a different stage for performing a second type of access"). See column 5, lines 24-29.

As per claim 6, Rangan teaches that the first type of access is a store access and the second type of access is a load access. See column 5, lines 24-29.

As per claim 7, Rangan teaches that the first type of access is a store access and the second type of access is a load (i.e. read) access. See column 5, lines 24-29.

As per claim 9, Rangan teaches comparing a new request with existing (i.e. older) access requests. See column 4, lines 30-32.

As per claim 11, Rangan teaches a cache memory 107 including a bank array 220 where each bank allows for one access each clock cycle (column 1, lines 21-23). A queue 210 stores each access request for the bank array ("storing access requests...to a pending request queue"),

and multiple ports from the queue may access the bank array. See column 1, lines 37-41, and column 3, lines 43-50. Rangan teaches conflict detection unit 240 which detects multiple requests in queue 210 to access the same bank in the bank array ("determining at least one access request in said pending request queue that has a bank conflict"). See column 4, lines 21-23. Rangan further teaches that entries in the queue may access the bank array in an out-of-order mode ("determining...that does not have a bank conflict). See column 3, lines 47-50. Since an entry in the queue may not issue until after the conflict is resolved (i.e. the older request has issued) and the queue is an out-of-order queue, then a newer entry will bypass the conflicting entry ("nominating...that does not have a bank conflict for issuance...").

Rangan does not teach determining bank conflict using virtual address bits instead of physical address bits. Rangan teaches accessing the L2 cache using physical addresses. Taylor et al. teaches a virtual cache, where the cache is accessed using virtual address bits instead of physical address bits. See column 2, lines 25-27. It would have been obvious to one of ordinary skill in the art to have modified Rangan to utilize a virtually accessed, L2 cache because Taylor et al. teaches that a virtual cache eliminates the need for a TLB in the cache of a cache hit, thus speeding up the memory access operation since the TLB translation does not need to be done before going to the cache. See column 2, lines 27-30.

As per claim 12, Rangan teaches issuing multiple requests stored in the queue 210 to the cache over a period of time. See column 3, lines 40-52.

As per claim 14, Rangan teaches comparing a new request for entry in the queue to existing queue entries. See column 4, lines 30-32.

As per claim 15, Rangan teaches a bank conflict with an existing queue entry, which is older than the new entry. See column 4, lines 36-39.

As per claim 16, Rangan teaches that the first type of access is a store access and the second type of access is a load access. See column 5, lines 24-29.

As per claim 17, Rangan teaches a pipeline, where one type of instruction is completed in stage X and another type of instruction is completed in stage X+2 ("a predefined pipeline...having a plurality of stages with one stage for performing a first type of access and a different stage for performing a second type of access"). See column 5, lines 24-29.

As per claim 18, Rangan teaches that the first type of access is a store access and the second type of access is a load (i.e. read) access. See column 5, lines 24-29.

### *Response to Arguments*

5. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

With respect to the Hetherington et al. reference, it is noted that the reference also teaches using virtual addresses (instead of physical addresses) to access the L2 cache. See column 13, lines 33-35.

### *Conclusion*

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(571) 273-4204**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (571) 272-4204. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (571) 272-4210.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
February 26, 2005